IN THE SPECIFICATION

Please enter the below claim amendments.

[0001] Current Memory Controller Hubs (MCHs) may be capable of supporting two memory channels, each of which may have up to four memory devices. The memory devices used in current computer systems may be memory modules packages, such as dual in line memory modules (DIMMs) or in the case of older computer systems the memory modules may be dynamic random access memories (DRAMS). Within each memory channel, a memory controller may populate the DIMMs in a specified order using a linear memory map. The memory control starts populating the memory modules starting with the memory module in the DIMM socket physically located farthest from the MCH on the channel. For example, if the DIMM sockets are numbered from 0 to 3, with the DIMM#3 being farthest from the MCH, the memory module in the DIMM#3 is populated first. Once the memory module in DIMM#3 is fully populated, then the next DIMM, DIMM#2, will be populated next, and so on. This places the load on the DIMMs as far from the MCH as possible. Because current memory controllers use memory addresses that are relative to a linear memory map and the physical memory arrangement of the DIMM is also linear, there is a one-to-one correspondence between the memory map and the physical memory arrangement.

[0006] The MCH 110 may contain a memory controller 115, which may be a double data rate (DDR) memory controller for direct-connection to a channel containing four DIMM devices. The memory controller 115 may perform a background data transfers between the locations in the DIMM memory modules 135, 140, 145, and 150, or from the memory modules in the DIMM memory modules 135, 140, 145, and 150 to a memory-mapped input/output (I/O) destination. The memory controller 115 may receive a logical address from the CPU 105 for data stored in or to be written to one of the DIMMs 135, 140, 145, and 150. The memory controller 115 may use a standard, predefined logic to fill the DIMMs 135, 140, 145, and 150 according to the logical address. For example, the memory controller 115 may populate DIMM #0 150 first, which is located farthest from the MCH 110. When all of the memory locations are filled in DIMM#0 150, the memory controller 115 may begin to fill the memory locations in the DIMM#1 145. Thus, the a logical chip select vectors may be used to fill the DIMM memory modules in a

sequential manner starting with the DIMM memory module farthest from the MCH 110. In one embodiment, the logical chip select vector is an array of all logical chip select bits.

[0008] The memory controller 115 transfers the logical CS vector to a Chip Set Remapping Logic Unit 120. The CS Remapping Logic Unit 120 takes the logical CS vector and generates an index value to lookup a corresponding physical CS vector. The logical vector may be a one-hot encoded vectors since any given memory transaction has a single physical target. The CS Remapping Logic Unit passes the logical CS vector through a one-hot index conversion process to generate an index value. The index values may be a sixteen (16) bit value, which may be used to access an appropriate physical CS vector from a soft table 130. The soft table 130 is accessible to the BIOS, and may be programmed to accommodate a number of different memory configurations. Each entry may contain the mapping definition for the logic to follow. To this end, each entry in the soft table 130 represents the physical CS vector to assert when that particular entry is selected by a particular index.

[0013] The logic circuit 200 may also contain a number of logical AND gates, which may be connected to the inputs 205, 210, 215, and 220. In an exemplary embodiment, the logic circuit may contain 16 logical AND gates 230, 232, 234, 236, 238, 240, 242,244, 246, 248, 250, 252, 254, 256, 258, and 260. Each of the input signals 205, 210, 215, and 220 may serve as one input to four separate logical AND gates. For example, input 205, may be mapped to logic AND gates 230, 238, 246, and 254, input 210 may be mapped to logic AND gates 232, 240, 248, and 256, while input 215 may be mapped to logic AND gates 234, 242, 250, and 258, and input 220 may be mapped to logic AND gates 236, 244, 252, and 260. The second input for each of the logic AND gates may be one of the 16 input lines 225.